## IN THE SPECIFICATION

Please amend the paragraph beginning on page 1, line 4, as follows:

This application is related to U.S. Patent Application No.[[ _____]] 10/643,741, entitled "Multistream Processing System and Method", filed on even date herewith; ~~to U.S. Patent Application No. _____, entitled "System and Method for Synchronizing Memory Transfers", Serial No. _____, filed on even date herewith;~~ to U.S. Patent Application No.[[ _____]] 10/643,742, entitled "Decoupled Store Address and Data in a Multiprocessor System", filed on even date herewith; to U.S. Patent Application No. [[_____]] 10/643,585, entitled "Latency Tolerant Distributed Shared Memory Multiprocessor Computer", filed on even date herewith; to U.S. Patent Application No. [[_____]] 10/643,754, entitled "Relaxed Memory Consistency Model", filed on even date herewith; to U.S. Patent Application No. [[_____]] 10/643,758, entitled "Remote Translation Mechanism for a Multinode System", filed on even date herewith; and to U.S. Patent Application No. [[_____]] 10/643,741, entitled "Method and Apparatus for Local Synchronizations in a Vector Processor System", filed on even date herewith, each of which is incorporated herein by reference.

Please amend the paragraph beginning on page 28, line 3, as follows:

For vector loads, the VU moves the memory data into the VR. For vector stores, the VU reads a VR and sends the store data to the EIU. The store address and data is sent decoupled to the EIU. This process is described in Patent application No. [[xx/yyy,yyy]] 10/643,742, entitled Decoupled Store Address and Data in A Multiprocessor System", filed herewith, the description of which is incorporated herein by reference.